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FPGA based seven-language electronic calendar for the revival of the cameroon culture

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Abstract

In this paper we present a device able to send information on time and date into seven languages (the two official languages of Cameroon English, French and five national languages of Cameroon Medumba, Ghomala, Yemba, Meta, Kom) to an LCD screen through a VGA controller. Hardware architecture is implemented on an Altera EP2C8Q208C8N FPGA (Field Programmable Gate Array) chip. The paper presents also the design of the top layer module of our system. Detailed information is focused on the system architecture. This calendar is developed using only the IEEE1164 standard hardware description language VHDL, to ensure the portability with any manufacturer. The system displays information in black color with a yellow background. The compiled design shows that the proposed algorithm gives good performance with short processing time (2 minutes and 54 seconds), low resource utilization (4000 logic elements, 1 PLL, 12 pins), small power consumption (111.03 mW) and memory usage (0 bit).

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Keywords: Calendar, FPGA, VHDL, National languages.

Résumé

Dans cet article nous présentons un dispositif capable d'envoyer les informations sur l'heure et la date en sept langues (les deux langues officielles du Cameroun Français, Anglais et cinq langues Nationales du Cameroun Medumba, Ghomala, Yemba, Meta, Kom) à un écran LCD pour affichage à travers un contrôler VGA. L'implémentation de l'architecture matérielle est faite en utilisant le composant FPGA (Field Programmable Gate Array) EP2C8Q208C8N d'Altéra. L'article présente aussi l'architecture matérielle globale des modules de notre système et les informations détaillées sur cette architecture. Le calendrier est développé en se basant sur le langage de description VHDL de la norme IEEE1164, pour en assurer la portabilité pour tous les fabricants. La date et l'heure sont affichées à l'écran en texte noir sur un fond jaune. Les résultats après compilation montrent que l'algorithme proposé donne une performance acceptable avec un temps de synthèse de l'implantation court (2 minutes et 54 secondes), l'utilisation des ressources minimale (4000 éléments logiques, 1 PLL, 12 broches), une consommation faible en énergie (111.03 mW) et en espace mémoire (0 bit).

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1. Introduction

During the last decade, much attention has been paid to language competition in complex systems community, that is, how the fractions of speakers of several competing languages evolve in time. In many countries, national languages are being introduced into the education curriculum encouraged by UNESCO [1]. These actions are taken to fight against causes that endanger languages as shown from a survey on previous studies on language competition. Around 50% of the 6000 languages spoken today are in danger and will disappear during the current century according to the recent studies in language contact [2]. Beyond Weinreich's Languages in contact [3], several studies in sociolinguistics have addressed questions regarding the level of endangerment of specific languages [4] and the challenge to find a common pattern that might relate language choice to ethnicity, community identity [5]. Finally, the need to provide a quantitative analysis in the field of sociolinguistics is getting an increasing attention [6]. This fact has triggered an effort in order to model and understand the mechanisms within scenarios of language competition: some models study the competition between many languages in order to reproduce the distribution of language sizes in the world in terms of the number of speakers [7, 8]; while others focus on the case of language contact between few languages (for a review see Refs [9, 10]). In particular, Abrams and Strogatz [11] proposed a simple mathematical model of competition between two languages. Recently, Patriarca and Castello [12] describe some modifications and extensions of Abrams and Strogatz model. From all these works, it has been shown that, the prestige of a language is very important when two languages are in competition. According to the value of the prestige of a language, this language can be extinct or coexist in competition.

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We used an Altera FPGA board to realize a seven-languages electronic calendar as our contribution to improve the prestige of some Cameroonian languages in competition with official languages. It is worth noting that, FPGA is being used to display on LCD screen, characters that are not found in the ASCII code, like characters of Chinese language [13]. We use the FPGA to realize our system because of the high processing speed that it offers, and which a microcontroller cannot achieve. Also our system has a VGA controller which is difficult to implement in a microcontroller. The motivations of this work are of three folds: a) Fighting against the growing death of Cameroonian languages, b) Adapting our culture to modern tools, c) Contributing to the socio-economic development of Cameroon by designing an apparatus that can help to program certain socio-cultural, commercial and administrative activities. The Altera's FPGA (EP2C8Q208C8N) is used as the core of the hardware circuit, we take the top-down programming methodology and adopt the integration tools (Quartus version 10.1 of Altera) [14] to design and implement the seven-language electronic calendar able to display time, days of week, month, and year in: English, French, Medumba, Ghomala, Yemba, Meta and Kom on an LCD screen. The originality of our work resides not only in the fact that we have used high level electronic design tools to realize this calendar but also in the fact that we are putting at the disposal of traditional rulers, cultural centers, local administration and traders, and population a working tool for their socio-cultural and socio-economic development. The calendar we propose is electronic, it can be used for long-range and short-range planning and offers more facilities than the hard calendar. Actually, UNESCO is funding research to fight against mother tongue extension. This fight will also be done with the introduction of mother tongue into ICT (Information Communication Technology). Our innovation begins the introduction of mother tongue into ICT.

The remainder of this paper is organized as follows. Section 2 introduces architecture of the electronic calendar, which includes the detailed design of hardware and software. The experimental results and analysis of the design are presented in Section 3 and some final conclusions and areas of future work are given in section 4.

2. System architecture

The electronic calendar is a digital system which utilizes top-down programming methodology according to hierarchy and functional separation [15]. Each functional module should be compiled and simulated, so the top-layer simulation of the electronic calendar can be passed without a hitch. The architecture of the electronic calendar system is shown in Figure 1. It consists of the following modules: PLL; VGA synchronization, Time clock and Character Generation Text. The Character Generation Text module is made of a Font ROM which is able to generate both African Characters as well as alphanumerical ones. In Figure1, the term Clock refers to the main clock signal coming from a 50MHz clock from the developing board Altera YG_V2.1; Reset is connected to high or low level. An ordinary VGA monitor contains 5 signals: R, G and B (tri-chromatic signal), then HS and VS for horizontal and vertical synchronization signals respectively [16]. All signals must meet requirements of the VGA monitor, and then the FPGA reads and display the information into an LCD (Liquid Crystal Display) monitor. It can display IPA (International Phonetic Alphabet) character according to the character generated by the Character Generation Text module. The Time Clock module generates the time and calculates the date to be displayed.

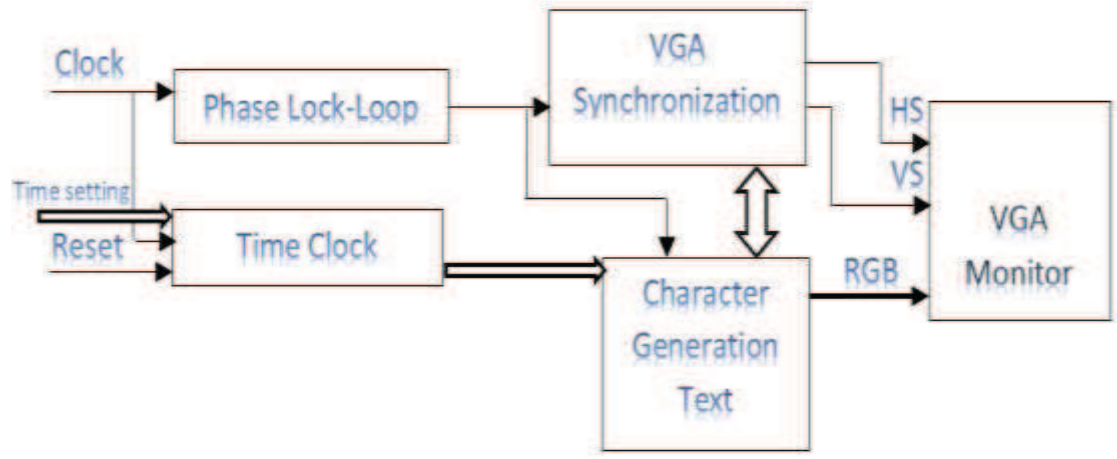

Figure 1. Architecture of the system.

2.1 Hardware design

The FPGA of Cyclone II family, named EP2C8Q208C8N produced by Altera is selected to realize the Multilingual Calendar. FPGA EP2C8Q208C8N is the core hardware of the system, which is responsible for the calendar implementation, the VGA Display and storage. EP2C8Q208C8N is a chip of 208 pins, among all the pins, 182 pins can be used as I/O pin at most, some of them can only act as input pin, some can be used as I/O port [17], Active Serial and JTAG configuration switched by special software. It has two PLL (Phase Locked Loop), 36 multipliers of 9-bit elements, 165888 total RAM bits and 8256 LE, each LE includes a LUT, a trigger and related relevant logic. Look-up table (LUT) is a RAM unit in fact. The whole design has been synthesized and implemented on Altera YG_V2.1 development board using Cyclone II FPGA. Here the Hardware architecture is coded in VHDL language using Altera Quartus II 10.1 compiler software.

2.2 Software design

This Multilingual Calendar is developed using only VHDL (hardware description language) based on the IEEE1164 standard, to ensure the portability with any manufacturer. The main modules include VGA synchronization module, Clock Timer, Character Generation Text and a PLL module. All modules are mutually independent, because working mode of FPGA is parallel. The following subsections delineate each of these blocks in details.

2.2.1. VGA Synchronization

The VGA Synchronization includes line synchronization signal (HS) and field synchronization signal (VS), these signals must be in strict accordance with the VGA timing standard. The video synchronization circuit generates the HS signal, which specifies the required time to traverse (scan) a row, and the VS signal, which specifies the required time to traverse (scan) the entire screen. Subsequent discussions are based on a 1024-by-768 VGA screen resolution with a 65MHz pixel rate [18], which means that 65M pixels are processed in a second. The screen of a LCD monitor usually includes a small black border and a middle rectangle visible portion. The coordinates of the top-left and bottom-right corners are (0, 0) and (1023, 767), respectively. The HS signal can be obtained by a special modulo-1344 counter and a decoding circuit. We start the counting from the beginning of the display region. This allows us to use the counter output as the horizontal (x-axis) coordinate. This output constitutes the vector-x signal. The HS signal goes low when the counter's output is between 1048 and 1184. Note that the LCD monitor should be black in the right and left borders and during retrace. We produce the h_video_on signal to indicate whether the current horizontal coordinate is in the displayable region. It is asserted only when the pixel count is smaller than 1024.

During the vertical scan, the electron beams move gradually from top to bottom and then return to the top. This corresponds to the time required to refresh the entire screen. The VS signal can be obtained by a special modulo-806 counter and a decoding circuit. Again, we start counting from the beginning of the display region. This allows us to use the counter output as the vertical (y-axis) coordinate. This output constitutes the vector-y signal. The VS signal goes low when the line count is between 771 and 777. As in the horizontal scan, we use the v_video_on signal to indicate whether the current vertical coordinate is in the displayable region. It is asserted only when the line count is smaller than 768. So the VGA Synchronization consists of the two counters for the horizontal and vertical scans [19]. We use two status signals, h_end and v_end, to indicate completion of the horizontal and vertical scans to the signal video_on.

2.2.2. Character Generation Text

The pixel generation circuit generates the 3-bit RGB signal for the VGA port. The external control and data signals specify the content of the screen, and the vector-x and vector-y signals from the VGA Synchronization module provides the current coordinates of the pixel. In our design, we are using two categories of pixel generation circuit which are bit-mapped scheme and tile-mapped scheme to realize the text generation module. In a bit-mapped scheme, a video memory is used to store the data to be displayed on the screen. Each pixel of the screen is mapped directly to a memory word, and the vector-x and vector-y signals form the address. A graphics processing circuit continuously updates the screen and writes relevant data to the video memory. The display scheme here, is made up of a collection of bits to form a tile and treat each tile as a display unit. The two schemes will be mixed together to generate a full screen. We have used a bit-mapped scheme to generate the background and tile-mapped to generate text for another part of the screen. For the text display, we use the 8-bit ASCII code for the character tiles. The patterns of the tiles constitute the font of the character set. We choose an 8-by-16 (i.e., 8-column-by-16-row) font similar to the one used in early IBM PC. The character patterns are stored in a ROM and each pattern requires 2^4 *8 bits. The pattern memory is known as font ROM. The original font set consists of 256 patterns, including digits, upper and lowercase letters, punctuation symbols, and many special purpose graphic

symbols. We implement only the first half [i.e., 128 (2^7)] of the patterns and replace most graphic symbols with some IPA characters. When we use these 8-by-16 characters (i.e., tiles) in a 1024-by-768 resolution screen, 128 tiles can be fitted into a horizontal line and 48 tiles can be fitted into a vertical line. We can put characters on the screen using these scaled coordinates. With this, the information's coming from the Clock Timer indicates the address of a tile to be displayed on the screen [20].

2.2.3. Clock Timer

The Clock Timer is the module that generates the information to be displayed on the screen. The clock signal of the board (50MHz) is divided by a frequency divider and produce a signal of 1 Hz, this signal of 1 Hz is then used to generate second, minute, hour, days, month and years count. A special sub module is used here to calculate the i^{th} day of the week in a system of seven days per week and a system of eight days per week.

2.2.4. PLL

The Pixel frequency being equal to 65MHz and the frequency of the clock of board being 50MHz, an electronic circuit is needed to multiply the clock of the board by a coefficient to produce the pixel frequency, therefore, one of the integrated PLL of the FPGA is used. The PLL is being generated from the software Quartus II and added to the top model as a component.

2.2.5. Top-layer diagram

The Top-layer Diagram is shown in Figure 2. PLL module (PLL:C0) generates 65MHz clock signal CLK. VGA_SYNC module generates vertical synchronisation, horizontal synchronisation and the coordinate of the pixel to ON or OFF. CLOCK_TIMER calculates and generates all the information about the date to be displayed. CHARACTER_GEN_TEXT generates the character to be displayed on the screen at the right position.

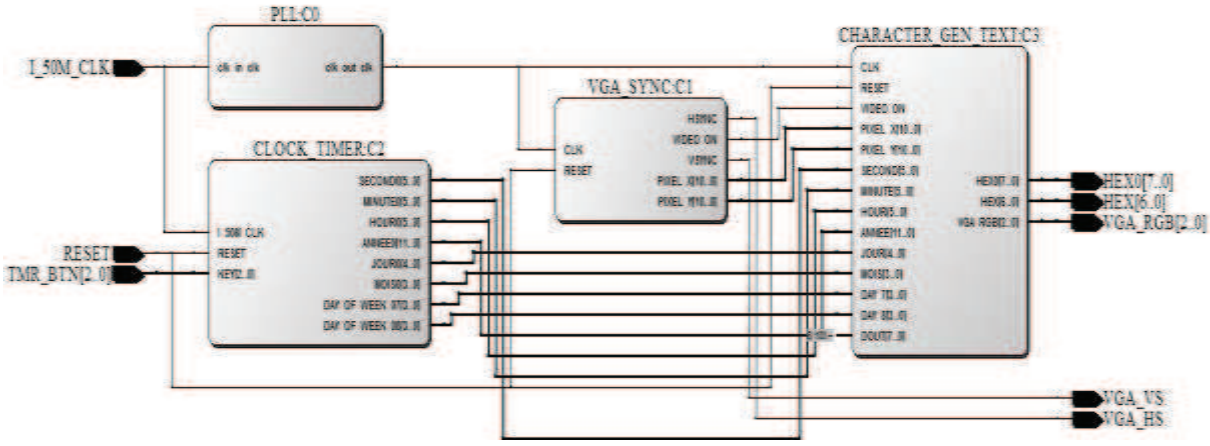

Figure 2. Top-layer Diagram.

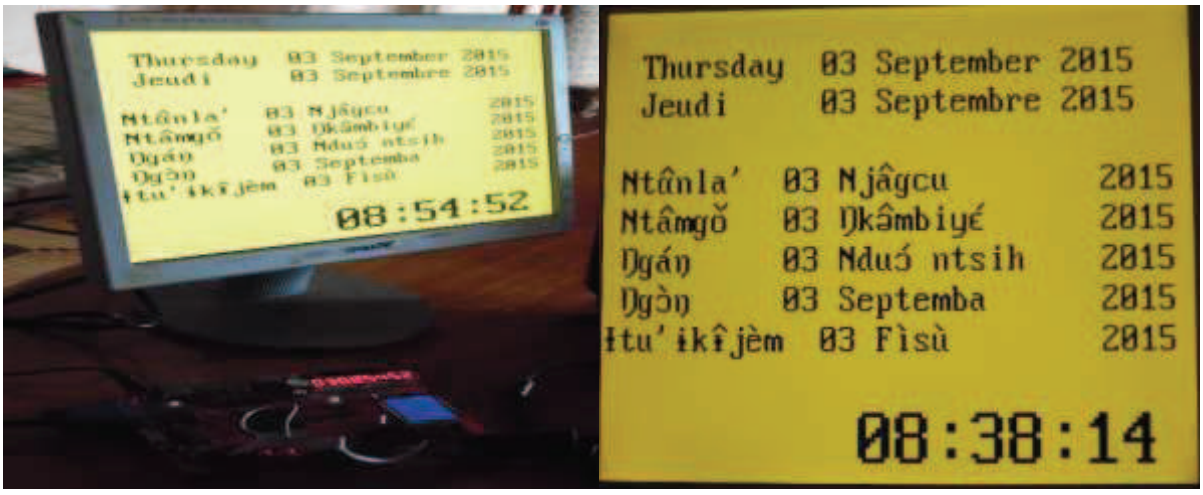

Figure 3. Experimental Setup and a zoom of the LCD Monitor showing Date and Time.

3. Experimental results and discussion

In order to be able to see the results obtained from the proposed algorithms on an FPGA, a standard VGA monitor may be chosen. The monitor used here is a VGA port LCD (Liquid Crystal Display). Procedure: Connect USB-Blaster between PC and experiment box; turn on power supply and select Programmer in Tools menu. Moreover, we should connect clock0 to 50MHz clock signal. If the above steps have been carried on, download the top layer file into the target device (EP2C8Q208C8N). After a successful downloading, the monitor displays the default date and the user can set the correct time and date using the up and down button of the selector. Figure 3 presents an example of the results where the order of languages is as stated in abstract.

From the experiment result, we can see that the benefits of using FPGA are obvious. In the process of system design and debugging, we can adjust or modify the system hardware at any time, but do not need to really change the ready-made board and the devices already soldered on the board. Modifications and adjustments can be made in the Altera Quartus II design environment. The use of a microcontroller to design this system could have not be an easy task from the hardware to the software. At the level of hardware, designing this system with microcontroller could having fastidious, the soldering of devices on the board and also to find a low cost microcontroller with a PLL able to generate 65 MHz needed to build the VGA controller for an LCD screen. But microcontroller can be used if the information is to be displayed to an LCD without VGA controller [21]. At the level of software, microcontroller execute instruction sequentially, so the programming language of this device does not admit structural description, then the designing will become complex in a system where time is to be calculated, generation of synchronization and characters at the same time, view the speed at which microcontrollers works. This electronic calendar is developed using only VHDL (hardware description language) based in the IEEE standards, where both behavioral and structural description can be used in designing to ensure the portability with any manufacturer. Our electronic calendar manufactured will be mobile and can be used on monitor having a VGA interface. This can lead to the diffusion of our national languages and also improve it prestige since, nowadays LCD monitor are cheap and can be easily found.

4. Conclusion and Future Work

In the proposed Electronic Calendar system, FPGA is used to develop this system, which can display date in seven languages and time. This architecture may be used in any FPGA device regardless of the brand or model. Experimental results show processing algorithms programmed in VHDL, which makes the design flexible and the programming very convenient. This design can be integrated in ICT devices, it can also be used to produce small size electronic device for giant calendar display via VGA port and others to fight against some causes that endangered African languages. In the future we can adopt more advanced ARM MCU (Acorn RISC Machine Microcontroller Unit) and FPGA chip to improve the feature of the calendar and even to add a sound module, so that the calendar should speaks.

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